Please amend the above-identified patent application as follows:

In the Claims

Please amend claim 1 as follows:

1. (Amended) A method for filling contact holes with metal by two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively;

filling a first metal layer into the first plurality of contact holes, entirely, so that the first metal layer is grown over and extends slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

Please add new claim 9 as follows:

9. (New) A method for filling contact holes with metal by a two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively;